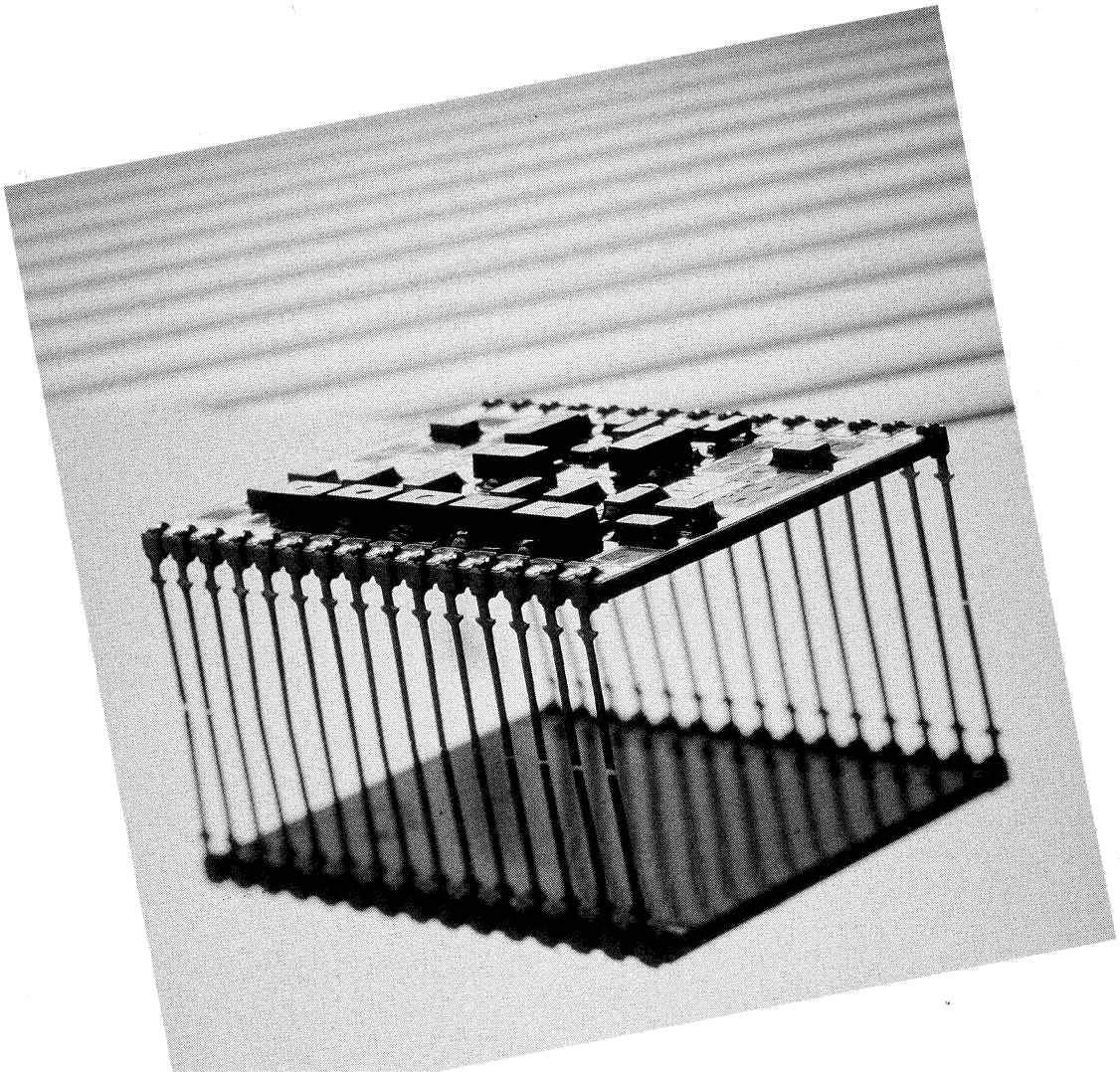
HEWLETT PACKARD

Synchronizing the HP 82000 to External Equipment

Application Note 390



Contents

For applications which involve testing either mixed analog and digital devices, or asynchronous devices, it is essential to synchronize the operation of the HP 82000 to signals generated by external apparatus. The synchronization requirements for an application like this are as follows:

1. Timing Synchronization.
The HP 82000 must generate and sample signals with a timing period set by an external clock source (bypassing the internal clock signal).

2. Phase Synchronization.
The generated and sampled signals must have a fixed phase-relationship to the external clock source - that is, there must be a constant delay between the occurrence of the clock signal and the execution of the first vector in the sequence of test data.

3. Event Synchronization.
The HP 82000 must be ready to generate/sample data at the instant that a triggering signal from the external source is received - to enable the test system to operate *coherently* when the system is used for asynchronous testing.

This Product Note describes:

* how the HP 82000 generates an internal reference clock;
* how to run the HP 82000 tester at the clock-frequency of an external piece of equipment;
* how to synchronize the edge-placement of the pin-drivers and receivers to a repetitive signal;
* how to trigger the Vector Sequencer from an external, asynchronous event, while maintaining timing-synchronization with an external clock.

The Timing Generator Circuitry

The master clock signal (MCLK) of the HP 82000 is produced by phase-locked-loop (PLL) using a crystal oscillator as its timing reference. The period of the MCLK signal is kept between 7.5 ns (133 MHz) and 5 ns (200 MHz). This signal is then distributed to the pin-drivers and receivers, where a frequency divider scales it to the value you have programmed in the Timing Setup screen. Figure 1-1 shows a simplified block diagram of the timing generator circuit.

Using an External Clock Source

When you select "clock source" as "extern" in the Timing Setup window, the PLL takes its timing reference from the signal fed to the "External Clock In" connector. You can scale the *actual* period of the external clock to the tester period *you need* by entering a ratio in the "external clock setup" screen. (It is worth reminding yourself that a *period* ratio of 1:2 is equivalent to a *frequency* ratio of 2:1!). Details of using the set up screen are given in Chapter 5 of *Using the HP 82000.*

Note that the "External Clock In" input is ac-coupled -- so make sure that the clock signal you feed to the BNC connector has a duty-cycle of around 50%!

Matching the Timing Setup Period and the External Clock Period

You must set the period entry in the Timing Setup window to match the period of your external clock as accurately as you can. This is a very important consideration, because the timing settings of the i/o channels are derived from the period settings that you enter. Any difference between the external clock period and the Timing Setup period is *directly* translated as an additional inaccuracy in the edge-delays that you have entered.

For example, with the period ratio set at 1:1, a 1% difference between the periods results in an additional 1% inaccuracy (over and above inaccuracy caused by the tester itself) of your programmed edge settings. A period ratio of 2:1 causes an additional inaccuracy of 2% at the DUT pins.

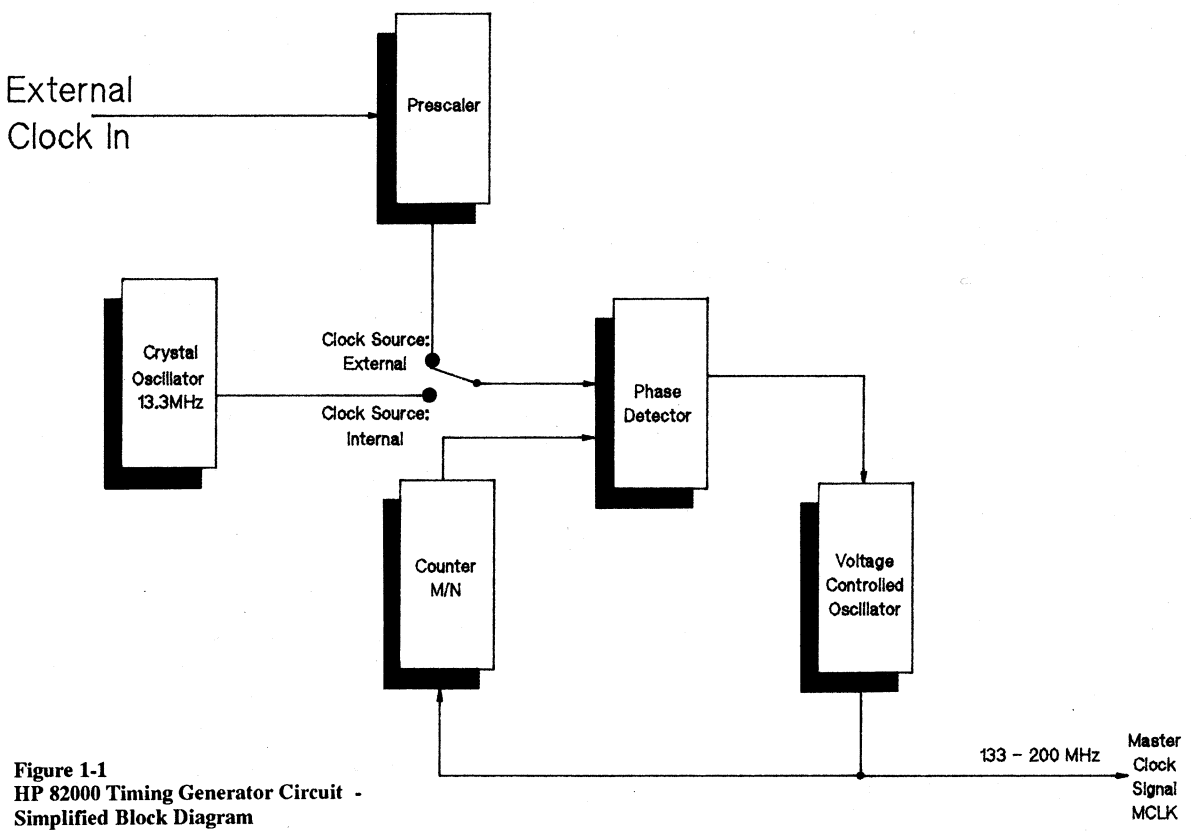


Figure 1-1
HP 82000 Timing Generator Circuit - Simplified Block Diagram

Synchronizing the Phase

Once the HP 82000 is locked onto the same frequency as your external clock-source, you can set the HP 82000 to generate/receive data at a selected phase of your external clock-source by feeding a second signal to the "External Sync In" connector. This input allows you to delay the drivers/receivers by between 0 and 999,999 ns in 50 ps increments up to a maximum delay of xxx ns. The delay is generated by a *skip* circuit (which ignores a discrete number of clock cycles) and an analog interpolator. The External Sync In connector is dc-coupled, and slope-sensitive.

You enter parameters for setting up the External Sync Input in the "external clock setup" screen. A full description is given in Chapter 5 of *Using the HP 82000.*

The External Sync feature is also useful when your external clock-source is running at a higher frequency than the testing frequency that you wish to use. For example, if you are testing a microprocessor with its own crystal-oscillator clock and a "divide by n" output pin, you can synchronize the HP 82000 to the "divide by n" phase by connecting this signal to the "External Sync In" connector.

If your external clock signal is at a frequency of less than 100 MHz, you can feed this same signal to both External Clock In and External Sync In.

Triggering the HP 82000 on an External Event

When you have set up the system to operate in synchronism with your external source, and at a set phase, you can use the Vector Sequencer to synchronize execution of your test vectors to a "Start of Test" signal. For this purpose, you use one of the "External Input" connectors, designated A and B on the mainframe front panel.

As well as a *running* state and a *break* state, the Vector Sequencer has a third operating state; *arm*. When you set the sequencer to *arm*, via the "Sequencer Programming" screen, the HP 82000 is held in a stand-by condition, with:

* the clock running at the required frequency and synchronized at the correct phase;

* no test being performed;

* no test vectors being output;

* the outputs held at the value entered in the "BreakVec" field of the Vector table.

When a signal is detected at the external input, the sequencer begins to execute the instructions in the test-cycle, and the test vectors are applied to the DUT. When the sequencer instructions have been completed, the HP 82000 returns to the "break" state. This gives a *One-Shot* operation of the test-cycle.

To set up a repetitive test-cycle, you can add a sequencer instruction to the end of your program to return the HP 82000 to the *arm* state at the beginning of the cycle, in preparation for the next "Start of Test" signal. In this type of application, the "Start of Test" trigger signal must appear only once during each cycle.

In your sequencer program, you must allow a waiting period to enable the external input to be detected. The length of this delay must be at least 10 cycles, plus the delay caused by the wiring to the DUT

The chapter "Vector Sequencer Programming" in *Advanced Testing with the HP 82000* gives more details about how to set up the external trigger inputs and how to use the *arm* state.

Further Considerations

Low-Pass Filter Effects

PLL circuits have another characteristic that you should consider when you use an external source. The VCO will respond to short term frequency changes in your external clock with a low-pass filter effect. This can produce a considerable amount of phase-jitter in the i/o driver channels of the HP 82000. This problem is unlikely to be significant if your external source is a crystal oscillator, but signal-generators or word-generators using RC or LC oscillators, or delay-line oscillators, can have poor timing stability.

Using the Trigger Out Socket

If your application requires an "End of Test" signal to be sent to the hardware, you can program the sequencer to output a signal when a particular vector in your test-cycle is reached. This signal is sent to the "Trigger Out" BNC connector on the mainframe.

Delays Due to Cable Lengths

The timing measurements of the HP 82000 are referenced to the inputs or outputs of the tester channels. In your timing calculations, you must make allowances for the additional delay caused by the wiring that you have added to the system.

To evaluate the timing characteristics of the HP 82000 using an external clock source, you can conduct this simple lab experiment. This procedure describes the use of Hewlett-Packard measurement equipment, but obviously, you can use any signal generator that you have available, for simulating the external clock-signal. A digital oscilloscope will also be needed, to monitor the synchronization of your external source with the HP 82000. The HP 82000 receives external synchronizing signals via BNC connectors mounted in the front panel of the mainframe. Figure 1-2. shows the positions of these connectors.

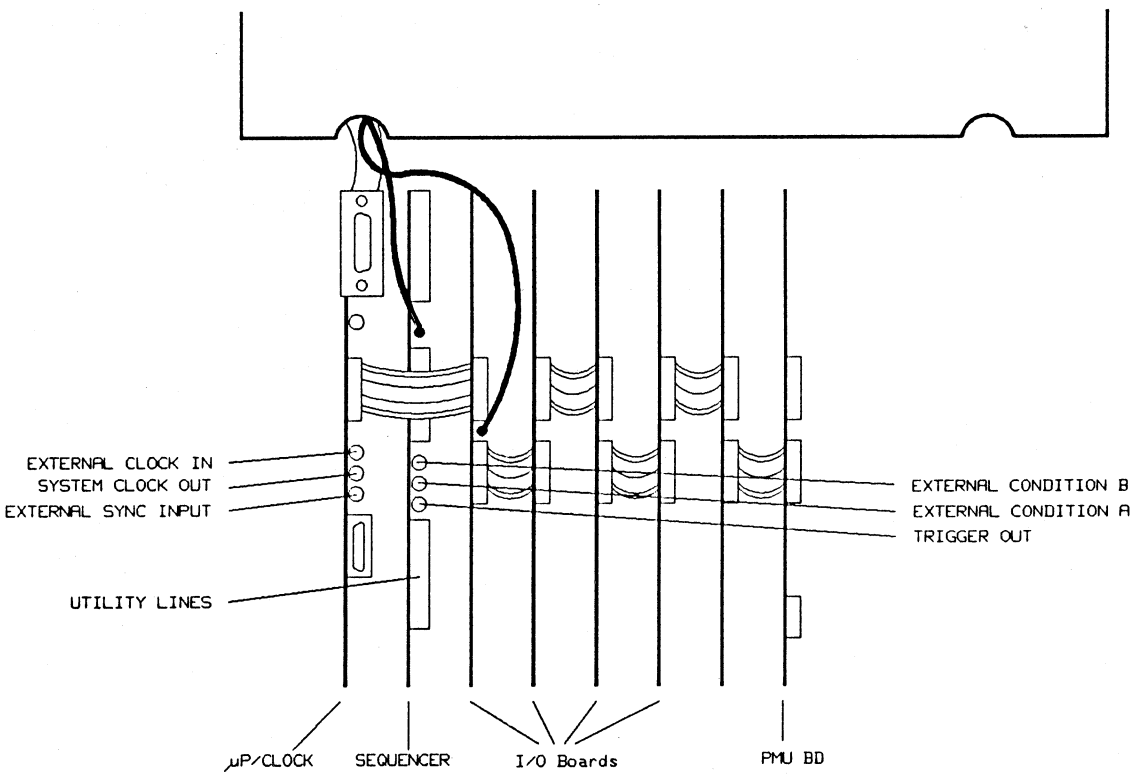


Figure 1-2.
Positions of the External Input Connectors Within Mainframe

Using an External Clock

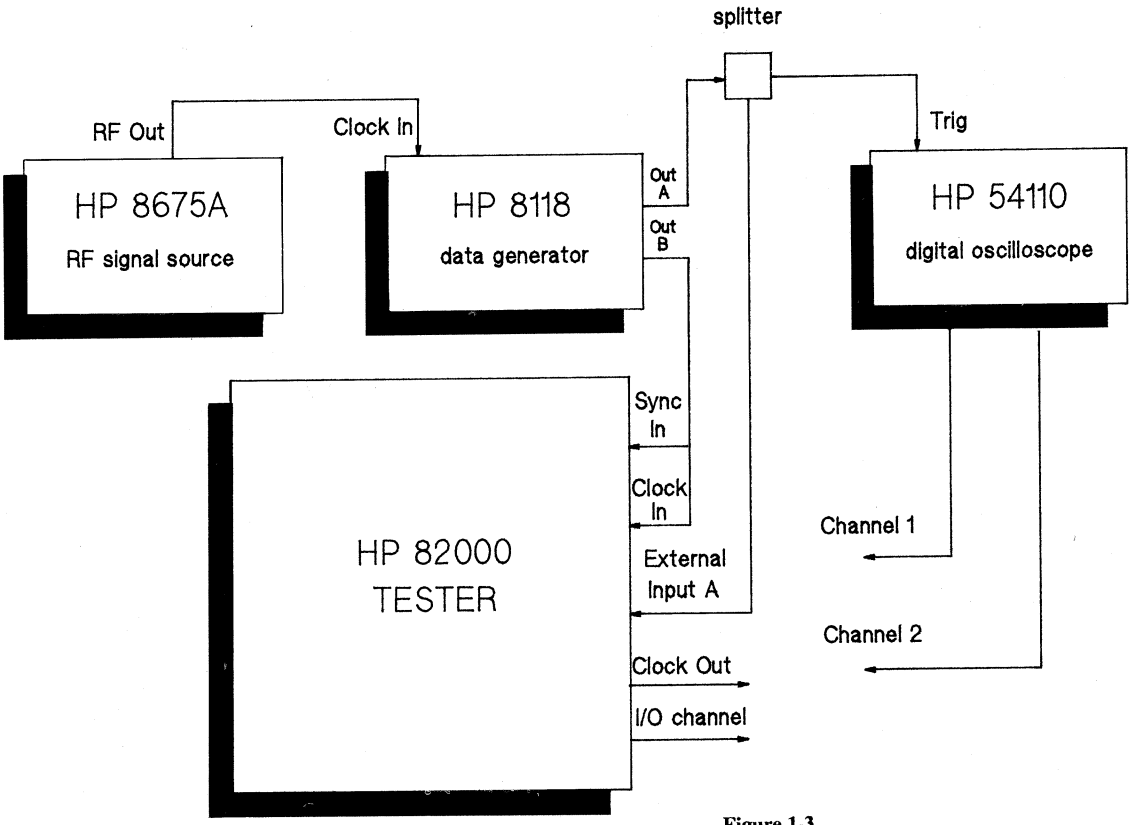


Figure 1-3.
Hardware Used in the External-Clocking Experiment

Set Up Procedure:

1. Set up the HP 82000 with your signal source and oscilloscope as shown in Figure 1-3.

2. In the Timing Setup window, set the clock source to "extern" and enter a timing period.

3. Adjust the frequency of the RF generator until the period of your external clock signal matches the period you have set in the Timing Setup window.

4. Connect the oscilloscope to the Clock Out connector on the mainframe front panel. (This allows you to observe the actual tester period being generated).

Observations
As you change the period of your external clock (i.e. the frequency of the RF generator), watch how the oscilloscope traces change.

When the difference between your external clock, and the period you

have set, exceeds a certain limit, the actual tester period (seen on the oscilloscope) is no longer the same as your programmed period.

This is the point at which the VCO reaches its frequency limit, and can no longer compensate the difference.

Set Up Procedure:

1. Set the RF source to a low-frequency (about 5 MHz).

2. Set the data generator to run with external clocking, and producing a 32-bit loop of return-to-zero (RZ) format signals with a symmetrical swing about 0V. Set the signal duty-cycle to 50%.

3. In the Pin Configuration window, define an input pin called "sync".

4. In the main Timing Setup window of the HP 82000:

* set the clock source to "external";

* set the period to 200 ns (a frequency of 5 MHz);

* set the format of "sync" as RZ.

5. In the "external clock setup" window of the Timing Setup window:

* set the period ratio to "1:1";

* set "synchronize to sync input signal" to the active state.

6. In the Vector Setup window, set up 16 vectors for "sync", with the drive data set to 0 for vectors 0 to 14, and vector 15 set to 1. Set the break vector to 0.

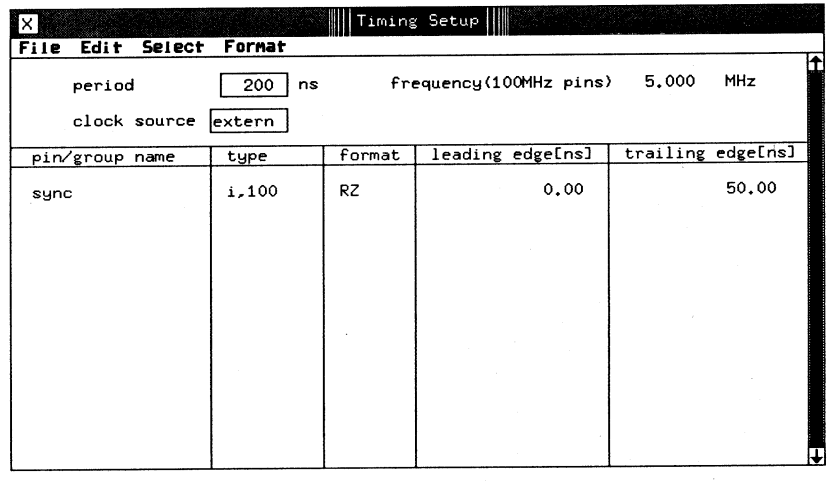


Figure 1-4.
Timing Setup

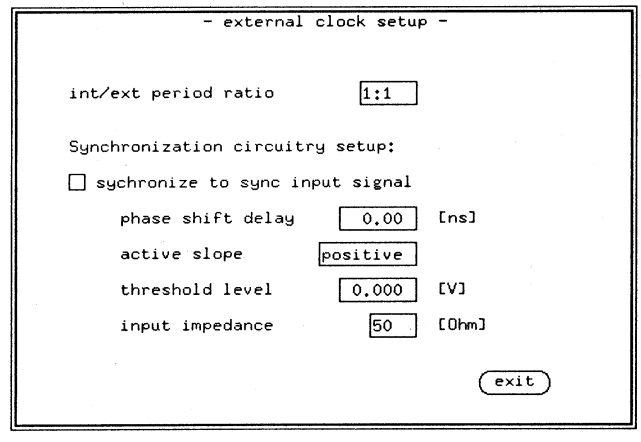


Figure 1-5.
External Clock Setup

Observations

Measure the delay between the Sync In signal and the DUT i/o pin.

Now, change the test period (and change the period of the external source accordingly) and notice that the delay between the Sync In signal and the output of the i/o pin remains *fixed.*

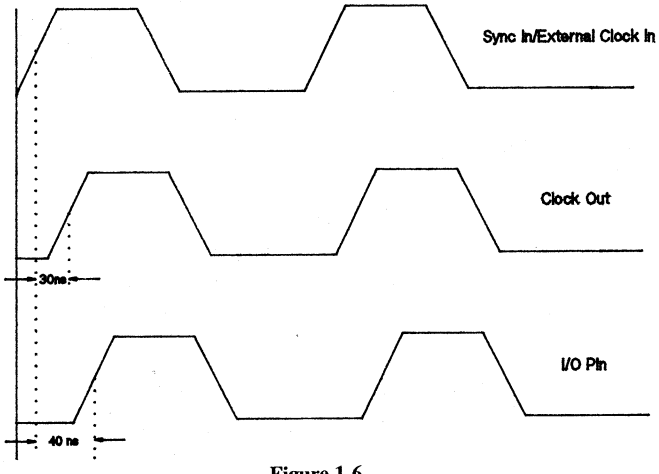


Figure 1-6.
Delay of I/O Pins and Clock Out Before Adding Programmed Delays

However, the value of the delay *is* affected by the actual calibration data being used.

In a single bay system with two i/o cards and a 900 mm cable set, this analog delay is approximately 40 ns. In a multibay system, the delay is about 55 ns.

You will see a similar, fixed delay between the Sync In signal and the clock output. The delay is about 30 ns.

By programming the synchronization delay in the "external clock setup" window, you can increase this 30 ns delay in steps of 50 ps. This delays the *occurrence* of the output edge with respect to the Sync In signal.

The delay of the Clock Out signal also follows the changes in the programmed delay settings.

Event Synchronization

Set Up Procedure:

1. In the "sequencer programming" screen (in the Vector Setup window):

* set the "arm on test execution" option at the top of the screen;

* set external input A to respond to a rising edge, and to trigger both jump and start;

* enter the following sequencer instructions:

2. Connect one oscilloscope channel to external input A, and the other to the pin "sync" at the DUT interface board

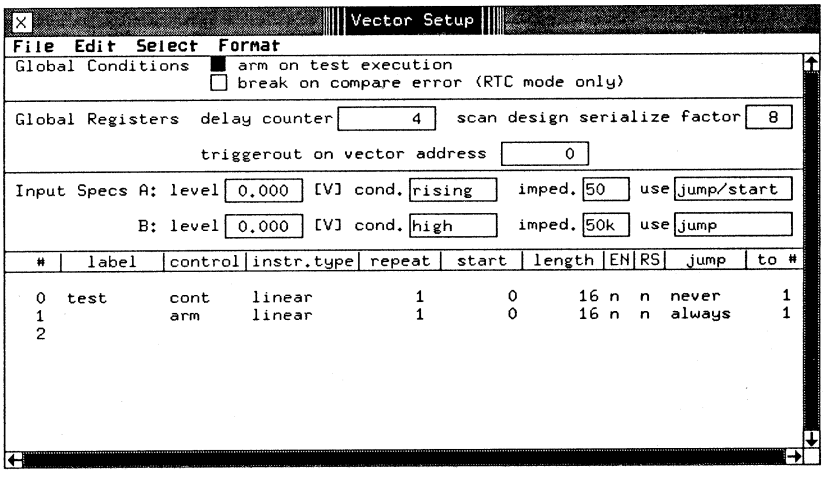


Figure 1-7.
Sequencer Program for Event Synchronization to External Input A

How The Sequencer Program Operates

When the label *test* is executed, the HP 82000 goes into the *arm* state. When a trigger event is detected at external input A, vectors 0 to 15 are executed.

Instruction #1 once more causes the HP 82000 to enter the *arm* state. When the next event is detected at external input A, vectors 0 to 15 are executed again, and the program jumps back to the beginning of instruction #1, where the system once more enters the *arm* state.

The program continues to loop through instruction #1, until you click the test function [BREAK] push button.

Sequencer Programming Considerations

* A minimum number of 8 vectors must be executed during each instruction of your vector program.

* The trigger signal must only occur once during each loop of the sequencer program - in other words, the repetition rate of the trigger must not exceed the rate at which the HP 82000 can execute the vector sequence and then return to the *arm* state.

* Due to internal pipeline delays, the HP 82000 requires 10 cycles in which to detect a trigger event at the external input A or B.

* To avoid break-cycles being inserted, the sequencer instructions should each execute a modulo-4 number of vectors.

Observations

Using the Sequencer Start option in the Test Control window, start the sequencer at the label "test".

On the oscilloscope you can see that the output of the i/o channel is in synchronism with the signals being fed to external input A.

You can observe that the input has a set-up time (t_{sup}) of approximately 6 ns with respect to the edge of the Sync In signal. The hold-time (t_{hold}) is approx 7 ns.

In other words, the trigger signal does not affect the timing of the output signal, as long as it meets the set-up/hold-time limits.

Making Measurements

All the measurements are taken on a typical system, and are made at the BNC sockets and at the DUT interface board. The cabling at the BNC sockets add an extra analog delay, which you must compensate for. Calibration and configuration of the system affect the delay between the synchronization signal and the i/o channel signals, but the value of this delay remains stable.

Using Additional Event Conditions

You can use several external-trigger events within your vector sequence. For example, you can use the second external input and the internal-triggering facilities of the HP 82000 to stop the test on a detected event. You can also use the "Trigger Out" BNC output to generate trigger signals for external equipment, thus closing the synchronization loop in the other direction.

Conclusion

Using the external-input facilities of the HP 82000, you can completely synchronize the operation of the system with externally-generated stimulus signals.

This allows you to use the HP 82000 in applications such as coherent sampling, and coherent data-generation, together with external analog or digital equipment.

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